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10/708,103	02/10/2004	Jacky Tsai	VIAP0083USA	2102

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NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
PEERS, CHASE W	
ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,103	TSAI, JACKY	
	Examiner	Art Unit	
	Chase Peers	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. As required by M.P.E.P. ' 201.14(c), acknowledgment is made of applicant's claim for priority based on an application filed in February 27, 2003.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contains subject matter that was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Lines 12-15 of Claim 1 and 15-18 of Claim 8 discloses *"comparing if at least one comparative bit of the given address matches those in any of the bit-patterns so as to determine the given address is located in one of the sections based on the comparison"*. The Examiner interprets this limitation to be claiming that if at least one comparative bit of the given address matches those in any of the bit-patterns, then it is determined the given address is located in the associated section.

The Examiner notes that Figure 5 and associated discussion in paragraph 34 of the specification disclose that to determine that an address is in a section each comparative bit of the address will need to match the bit-mask. Paragraph 34 discloses

that comparison unit 112C will output a result of "true" to reflect the fact that the given address is located in the memory module 80D, but if the claimed test *"if at least one comparative bit of the given address matches those in any of the bit-patterns"* is used then each of the comparison units will output a result of "true", in that bit 31 ('0') of the address matches bit 31 of each of the bit-patterns.

This rejection may be withdrawn pending further clarification or amending Claim 1 limitations to read "*comparing the given address against any of the bit-patterns so as to determine the given address is located in one of the sections based on the comparison*".

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-11 are rejected under 35 U.S.C. 101 because the claimed inventions are directed to non-statutory subject matter.

3. As per claim 1, the claimed inventions are directed towards an abstract idea, per se, but do not transform an article or physical object to a different state or thing and do not produce a tangible result. To direct the claimed inventions to statutory subject matter, the claims must be amended to include performing a physical transformation that produces a tangible result, such as storing the corresponding address, the single bit-pattern or the result of the determination in a memory.

4. As per claims 2-11, the additional limitations disclosed do not direct the claimed inventions towards statutory subject matter. To direct the claimed inventions to statutory subject matter, the Examiner directs the applicant to the 35 U.S.C. 101 rejection of claim 1 above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koos (Pat No 4400794) in view of Schmisseur et al. (Pat No 6,128,718).

5. Regarding claims 1, 2 and 4, Koos discloses a memory address decoding method for determining if a given address (memory address location, column 1 line 22) is located in one of a plurality of sections (memory boards, column 1 line 13), each section having a plurality of memory units and each memory unit having a unique corresponding address (memory locations, column 1 line 18), the corresponding address using the binary system (column 1 lines 39-44), the method comprising: determining if the given address is located in one of the sections (column 3 lines 20-62).

Koos does not disclose building a single bit-pattern for each section from all corresponding addresses; and comparing if at least one comparative bit of the given

address matches those in any of the bit-patterns so as to determine the given address is located in one of the sections based on the comparison.

Schmisseur discloses building a single bit-pattern ("a single bit-pattern" is interpreted to be claiming exactly one bit-pattern, as opposed to a pattern consisting of a single bit) for each section from all corresponding addresses (column 4, lines 55-59); and if the comparative bits (additional addressing bits, column 4 line 65) of the given address matches those in a bit-pattern, the given address is located in the section based on the comparison (column 4, lines 55-59).

Koos and Schmisseur are analogous art in that they both deal with memory mapping and addressing. Koos and Schmisseur are analogous art in that Koos and Schmisseur deal with prefix addresses for a plurality of differently sized memories. The likelihood that an address is in a given memory is proportional to its size compared to the entire addressable memory space. Differently sized memories are analogous to elements of different probability in that a memories size will take up a portion of the total addressable space, and an element's probability will take up a portion of the total probability space.

At the time of the invention it would have been obvious to one with ordinary skill in the art to modify the memory mapping system taught by Koos to assign memory ranges using Schmisseur's prefix codes. The motivation for using Schmisseur's prefix codes would have been that only a portion of the address must be examined to determine if an address is in a memory section (column 4, lines 51-62), where Koos teaches performing processing on the entire address (figure 2). Therefore, it would have

been obvious to combine the memory mapping of Koos with Schmisseur's prefix codes for the benefit of examining only a portion of the address and for minimizing that portion, to obtain the invention of claims 1, 2 and 4.

Claim 3 rejected under 35 U.S.C. 103(a) as being unpatentable over Koos and Schmisseur et al. as applied to claim 1 above, and further in view of Nunziata (Pat No 5737572).

6. Koos and Schmisseur et al. describe all the limitations of claim 1, but do not expressly disclose the sections are a plurality of rank memory arrays and an even number of rank memory arrays of the same size compose a memory module.

Nunziata does disclose the sections being a plurality of rank memory arrays and an even number of rank memory arrays of the same size compose a memory module (Column 1, lines 30-65 and figure 4).

Koos, Schmisseur et al. and Nunziata are analogous art because they are from the same field of endeavor, memory management. At the time of the invention it would have been obvious to a person of ordinary skill in the art to have the sections in memory be rank memory arrays and have an even number of them. The suggestion for doing so would have been that it is an easy way to address memory and is the de facto standard in the industry. Therefore, it would have been obvious to combine Koos, Schmisseur et al. and Nunziata for the benefit of ease of use and standardization to obtain the invention as specified in claim 3.

Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Koos and Schmisseur et al. as applied to claims 1 and 4 above, and further in view of Srinivasan et al. (Pat No 6219748).

7. Regarding claim 5, Koos and Schmisseur et al. describe all of the limitations of claims 1 and 4, but do not expressly describe that if the comparative bits do not completely match all the bit-patterns of any of the sections, the given address is not located in the section.

Srinivasan et al. does disclose that if the comparative bits do not completely match all the bit-patterns of any of the sections, the given address is not located in the section (Column 15, lines 9-45).

Koos, Schmisseur et al. and Srinivasan et al. are analogous art because they are from the same field of endeavor, memory management. At the time of the invention it would have been obvious to a person of ordinary skill in the art to say that the address is not located in the section if the comparative bits don't match. The suggestion for doing so would have been to not waste time by searching for a partial match. Therefore, it would have been obvious to combine Koos, Schmisseur et al. and Srinivasan et al. for the benefit of saving time to obtain the invention as specified in claim 5.

Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Koos and Schmisseur et al. as applied to claims 1 and 4 above, and further in view of Stewart et al. (Pat No 4914577).

8. Regarding claim 6, Koos and Schmisseur et al. describe all of the limitations of claims 1 and 4, but do not expressly describe that if the comparative bits of the given address match the bit pattern of one section, the given address is not greater than the largest address in the section.

Stewart et al. does disclose that if the comparative bits of the given address match the bit pattern of one section, the given address is not greater than the largest address in the section (column 13, lines 30-44).

Koos, Schmisseur et al. and Stewart et al. are analogous art because they are from the same field of endeavor, memory management. At the time of the invention it would have been obvious to a person of ordinary skill in the art to make a system where a given address is smaller than the largest address in a section, which is inherent in a associative memory system. The suggestion for doing so would have been increased memory efficiency. Therefore, it would have been obvious to combine Koos, Schmisseur et al. and Stewart et al. for the benefit of memory efficiency to obtain the invention as specified in claim 6.

Claim 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Koos, Schmisseur et al., and Stewart et al. as applied to claims 1, 4, and 6 above, and further in view of Sherman (Par 6389507).

9. Regarding claim 7, Koos, Schmisseur et al. and Stewart et al. describe all of the limitations of claims 1, 4 and 6, but do not expressly describe determining the given address is located in one of the sections based on the comparison comprises searching

for the sections which one of its bit-patterns matches the comparative bits, and judging the given address is located in one section which the greatest corresponding address is the smallest.

Sherman discloses determining the given address is located in one of the sections based on the comparison comprises searching for the sections which one of its bit-patterns matches the comparative bits, and judging the given address is located in one section which the greatest corresponding address is the smallest (column 3 line 49 to column 4 line 9).

Koos, Schmisseur et al., Stewart et al. and Sherman are analogous art because they are from the same field of endeavor, memory management. At the time of the invention it would have been obvious to a person of ordinary skill in the art to determine where an address is by use of a tree structure and determining likelihood at each node. The suggestion for doing so would have been to decrease the number of transistors on the CAM and allow for more room for storage. Therefore, it would have been obvious to combine Koos, Schmisseur et al., Stewart et al. and Sherman for the benefit of efficiency to obtain the invention as specified in claim 7.

Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Koos and Schmisseur et al. as applied to claim 1 above, and further in view of Yoshioka et al. (5835963).

10. Koos and Schmisseur et al. describe all the limitations of claim 1, but do not expressly disclose that the bit-patterns consisting of partial common bits of the corresponding addresses in each section.

Yoshioka et al. does disclose the bit-patterns consisting of partial common bits of the corresponding addresses in each section (column 4, lines 1-29).

Koos, Schmisseur et al., and Yoshioka et al. are analogous art because they are from the same field of endeavor, memory management. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use some common bits of the corresponding address. The suggestion for doing so would have been to standardize access to the cache and TLB. Therefore, it would have been obvious to combine Koos, Schmisseur et al., and Yoshioka et al. for the benefit of access standardization to obtain the invention as specified in claim 8.

Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Koos, Schmisseur et al., and Yoshioka et al. as applied to claims 1 and 8 above, and further in view of Srinivasan et al. (Pat No 6219748).

11. Regarding claim 9, Koos, Schmisseur et al., and Yoshioka et al. describe all of the limitations of claims 1 and 8, but do not expressly describe that if the comparative bits do not completely match all the bit-patterns of any of the sections, the given address is not located in the section.

Srinivasan et al. does disclose that if the comparative bits do not completely match all the bit-patterns of any of the sections, the given address is not located in the section (Column 15, lines 9-45).

Koos, Schmisseur et al., Yoshioka et al. and Srinivasan et al. are analogous art because they are from the same field of endeavor, memory management. At the time of the invention it would have been obvious to a person of ordinary skill in the art to say that the address is not located in the section if the comparative bits don't match. The suggestion for doing so would have been to not waste time by searching for a partial match. Therefore, it would have been obvious to combine Koos, Schmisseur et al., Yoshioka et al. and Srinivasan et al. for the benefit of saving time to obtain the invention as specified in claim 9.

Claim 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Koos, Schmisseur et al., Yoshioka et al. and Srinivasan et al. as applied to claims 1, 8, and 9 above, and further in view of Stewart et al. (Pat No 4914577).

12. Regarding claim 10, Koos, Schmisseur et al., Yoshioka et al. and Srinivasan et al. describe all of the limitations of claims 1 and 4, but do not expressly describe that if the comparative bits of the given address match the bit pattern of one section, the given address is not greater than the largest address in the section.

Stewart et al. does disclose that if the comparative bits of the given address match the bit pattern of one section, the given address is not greater than the largest address in the section (column 13, lines 30-44).

Koos, Schmisseur et al., Yoshioka et al., Srinivasan et al. and Stewart et al. are analogous art because they are from the same field of endeavor, memory management. At the time of the invention it would have been obvious to a person of ordinary skill in the art to make a system where a given address is smaller than the largest address in a section, which is inherent in a associative memory system. The suggestion for doing so would have been increased memory efficiency. Therefore, it would have been obvious to combine Koos, Schmisseur et al., Yoshioka et al., Srinivasan et al. and Stewart et al. for the benefit of memory efficiency to obtain the invention as specified in claim 10.

Claim 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Koos, Schmisseur et al., Yoshioka et al., Srinivasan et al. and Stewart et al. as applied to claims 1 and 8-10 above, and further in view of Sherman (Par 6389507).

13. Regarding claim 11, Koos, Schmisseur et al., Yoshioka et al., Srinivasan et al. and Stewart et al. describe all of the limitations of claims 1 and 8-10, but do not expressly describe determining the given address is located in one of the sections based on the comparison comprises searching for the sections which one of its bit-patterns matches the comparative bits, and judging the given address is located in one section which the greatest corresponding address is the smallest.

Sherman discloses determining the given address is located in one of the sections based on the comparison comprises searching for the sections which one of its bit-patterns matches the comparative bits, and judging the given address is located in

one section which the greatest corresponding address is the smallest (column 3 line 49 to column 4 line 9).

Koos, Schmisseur et al., Yoshioka et al., Srinivasan et al., Stewart et al. and Sherman are analogous art because they are from the same field of endeavor, memory management. At the time of the invention it would have been obvious to a person of ordinary skill in the art to determine where an address is by use of a tree structure and determining likelihood at each node. The suggestion for doing so would have been to decrease the number of transistors on the CAM and allow for more room for storage. Therefore, it would have been obvious to combine Koos, Schmisseur et al., Yoshioka et al., Srinivasan et al., Stewart et al. and Sherman for the benefit of efficiency to obtain the invention as specified in claim 11.

Claims 12-14, and 16 rejected under 35 U.S.C. 103(a) as being unpatentable over Koos and further in view of Schmisseur et al. and Wan (Pat No 5710905).

14. Regarding claims 12-14 and 16, Koos discloses a memory address decoding method for determining if a given address (memory address location, column 1, line 22) is located in one of a plurality of sections (memory boards, column 1, line 13), an access module for receiving addresses (column 2, lines 1-11), each section having a plurality of memory units and each memory unit having a unique corresponding address (memory locations, column 1, line 18), the corresponding address using the binary system (column 1, lines 39-44), the method comprising: determining if the given address is located in one of the sections (column 3, lines 20-62).

Koos does not disclose building a single bit-pattern for each section from all corresponding addresses, comparing if at least one comparative bit of the given address matches those in any of the bit-patterns so as to determine the given address is located in one of the sections based on the comparison, or a pattern calculation module

Schmisseur et al. discloses building a single bit-pattern ("a single bit-pattern" is interpreted to be claiming exactly one bit-pattern, as opposed to a pattern consisting of a single bit) for each section from all corresponding addresses (column 4, lines 55-59); and if the comparative bits (additional addressing bits, column 4 line 65) of the given address matches those in a bit-pattern, the given address is located in the section based on the comparison (column 4, lines 55-59).

Koos and Schmisseur et al. are analogous art in that they both deal with memory mapping and addressing. Koos and Schmisseur et al. are analogous art in that Koos and Schmisseur et al. deal with prefix addresses for a plurality of differently sized memories. The likelihood that an address is in a given memory is proportional to its size compared to the entire addressable memory space. Differently sized memories are analogous to elements of different probability in that a memories size will take up a portion of the total addressable space, and an element's probability will take up a portion of the total probability space.

At the time of the invention it would have been obvious to one with ordinary skill in the art to modify the memory mapping system taught by Koos to assign memory ranges using Schmisseur's prefix codes. The motivation for using Schmisseur's prefix

codes would have been that only a portion of the address must be examined to determine if an address is in a memory section (column 4, lines 51-62), where Koos teaches performing processing on the entire address (figure 2). Therefore, it would have been obvious to combine the memory mapping of Koos with Schmisseur's prefix codes for the benefit of examining only a portion of the address and for minimizing that portion.

Koos and Schmisseur et al. describe the limitations above, but don't expressly describe a pattern calculation module for building at least one bit-pattern for each section based on the corresponding addresses, a logic module responsible for receiving the comparison signals, sending a decoding result for determining the given address is located in one of sections or the sections are a plurality of memory modules.

Wan does describe a pattern calculation module for building at least one bit-pattern for each section based on the corresponding addresses, a logic module responsible for receiving the comparison signals, sending a decoding result for determining the given address is located in one of sections or the sections are a plurality of memory modules (abstract, column 5, lines 36-44, and column 5 line 65 to column 6 line 4).

Koos, Schmisseur et al. and Wan are analogous art because they are from the same field of endeavor, memory management. At the time of the invention it would have been obvious to a person of ordinary skill in the art to have a module to make a pattern, receive comparison signals, and send the result for determining. The suggestion for doing so would have been to have a more efficient cache and higher memory cache system. Therefore, it would have been obvious to combine Koos, Schmisseur et al. and

Wan for the benefit of efficiency to obtain the invention as specified in claim 12-14 and 16.

Claim 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Koos, Schmisseur et al. and Wan as applied to claim 12 above, and further in view of Nunziata.

15. Koos, Schmisseur et al. and Wan describe all the limitations of claim 1, but do not expressly disclose the sections are a plurality of rank memory arrays and an even number of rank memory arrays of the same size compose a memory module.

Nunziata does disclose the sections being a plurality of rank memory arrays and an even number of rank memory arrays of the same size compose a memory module (Column 1, lines 30-65 and figure 4).

Koos, Schmisseur et al., Wan and Nunziata are analogous art because they are from the same field of endeavor, memory management. At the time of the invention it would have been obvious to a person of ordinary skill in the art to have the sections in memory be rank memory arrays and have an even number of them. The suggestion for doing so would have been that it is an easy way to address memory and is the de facto standard in the industry. Therefore, it would have been obvious to combine Koos, Schmisseur et al., Wan and Nunziata for the benefit of ease of use and standardization to obtain the invention as specified in claim 15.

Claim 17 rejected under 35 U.S.C. 103(a) as being unpatentable over Koos, Schmisseur et al. and Wan as applied to claim 12 above, and further in view of Yoshioka et al.

16. Koos, Schmisseur et al. and Wan describe all the limitations of claim 1, but do not expressly disclose that the bit-patterns consisting of partial common bits of the corresponding addresses in each section.

Yoshioka et al. does disclose the bit-patterns consisting of partial common bits of the corresponding addresses in each section (column 4, lines 1-29).

Koos, Schmisseur et al., Wan and Yoshioka et al. are analogous art because they are from the same field of endeavor, memory management. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use some common bits of the corresponding address. The suggestion for doing so would have been to standardize access to the cache and TLB. Therefore, it would have been obvious to combine Koos, Schmisseur et al., Wan and Yoshioka et al. for the benefit of access standardization to obtain the invention as specified in claim 17.

Allowable Subject Matter

Claim 18 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chase Peers whose telephone number is (571) 272-6757. The examiner can normally be reached on from Monday to Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PIERRE BATAILLE
PRIMARY EXAMINER
4/2/06